WHAT IS CLAIMED IS:

1. A method for designing a semiconductor integrated circuit comprising basic elements and wirings connecting the basic elements, the method comprising:

a first timing verification procedure for verifying the timing between flip–flops by adding delay times of the basic elements and the wirings;

a slack sort procedure for extracting flip–flops at the starting point and the end point of a path, a delay time and a set–up time of cells constituting the path, and a slack with respect to a cycle time from a timing report output by the first timing verification procedure;

a flip–flop driving ability change procedure for substituting a flip–flop having a delay time larger than a transition time from a state in which a power supply voltage drops due to a resistance component of a power supply wiring to a state of an ideal power supply for an arbitrary flip–flop;

a layout modification procedure for allowing a netlist modified by the substitution to be reflected on the layout;

a delay calculation procedure for calculating a delay from a delay library of only the flip–flops taking a voltage drop into consideration and a delay library produced in a state of an ideal power supply voltage; and

a second timing verification procedure for verifying a timing using delay information output from the delay calculation procedure.

2. A method for designing a semiconductor integrated circuit comprising basic elements and wirings connecting between the basic elements, the method comprising:

a first timing verification procedure for verifying the timing between flip–flops by adding delay times of the basic elements and the wirings;

a slack sort procedure for extracting flip–flops at the starting point and the end point of a path, and a slack with respect to a cycle time of the path from a timing report output by the first timing verification procedure;

a positive/negative flip–flop change procedure for substituting a flip–flop operating at the trailing edge of the clock signal for a flip–flop operating at the rising edge of the clock signal at the end point of the path whose slack is larger than 1/2 of the cycle time so as to make more uniform an amount of a voltage drop at the power supply voltage due to a resistance component of the power supply wiring;

a layout modification procedure for allowing a netlist modified by the substitution to be reflected on the layout;

a delay calculation procedure for calculating a delay from a delay library corresponding to the more uniform amount of the voltage drop; and

a second timing verification procedure for verifying a timing using delay information output from the delay calculation procedure.

3. A method for designing a semiconductor integrated circuit comprising basic elements and wirings connecting between the basic elements, the method comprising:

a first timing verification procedure for verifying the timing between flip–flops by adding delay times of the basic elements and the wirings;

a slack sort procedure for extracting flip–flops at the starting point and the end point of a path and a slack with respect to a cycle time of the path from a timing report output by the first timing verification procedure;

a flip–flop substitution procedure for substituting a buffer having a delay time that is the same as the total time of a set–up time, a delay time of a flip–flop and the slack for the flip–flop at the end of the path whose slack is approximate to zero;

a layout modification procedure for allowing a netlist modified by the substitution to be reflected on the layout;

a delay calculation procedure for calculating a delay from a delay library produced in a state of an ideal power supply voltage; and

a second timing verification procedure for verifying the timing using delay information output from the delay calculation procedure.